RESEARCH ARTICLE

OPEN ACCESS

Comparison of Performance of VSI and Z-Source Inverter for **Space Vector PWM**

E. Sai Prateek¹, Ashmeet Kandhari², Ch. Chenchu Kalyan Chakravarthy³, T Nithin Krishna⁴, K.Dinesh⁵

Dept of EEE, KL University, Vaddeswaram, Guntur, A.P., India

Abstract

Z-Source Inverters have the ability to boost the dc link voltage, thus increasing the output ac voltage beyond the values reached by conventional inverters. The enhanced ratio from ac output voltage to dc link voltage is possible due to an impedance network connected between the dc power supply and the main converter. The space vector pulse width modulation techniques gives more dc bus utilisation and low harmonics than other pulse width modulation techniques. In this paper space vector pwm is implemented for conventional VSI and Zsource inverter. The results are supported by SIMULINK simulation

keywords: voltage source inverters, z-source, spece vector, low harmonics, dc bus utilisation

I. INTRODUCTION

Voltage Source Inverters (VSI) controlled by Space Vector Modulators (SVM) produce output voltages whose fundamental amplitude is given by[6]

 $Vs = \frac{M}{\sqrt{2}} * Vdc$

Where M- modulation index

Vdc- DC link voltage

The maximum amplitude is given by $Vs = \frac{vdc}{\sqrt{3}} = 0.57*Vdc$ when m=1

On the other hand, Z-Source Inverters (ZSI) produce output voltages that are higher than those obtained by the Voltage source inverter

Vzs,max > Vs,max

with the same VDc. This is the main advantage of this configuration.

The intermediate circuit of the ZSI is composed by two inductors, L z, two capacitors, and a diode D z, see Fig. 2. Assuming that both inductors have the same inductance, and both capacitors have the same capacitance, the order of the differential equations can be reduced in two. The state variables of the intermediate circuit are iz and v z. The inverter is a two-level VSI formed by six IGBTs. The load is a three phase RL circuit.







Fig.2 Z source three phase VSI

II. SPACE VECTOR PULSE WIDTH MODULATION

Space vector modulation is a PWM control algorithm for multi-phase AC generation, in which the reference signal is sampled regularly; after each sample, non-zero active switching vectors adjacent to the reference vector and one or more of the zero switching vectors are selected for the appropriate fraction of the sampling period in order to synthesize the reference signal as the average of the used vectors. The topology of a three-leg voltage source inverter is Because of the constraint that the input lines must never be shorted and the output current must always be continuous a voltage source inverter can assume only eight distinct topologies. Six out of these eight topologies produce a nonzero output voltage and are known as non-zero switching states and the remaining two topologies produce zero output voltage and are known as zero switching states.

STEPS TO IMPLEMENT SVPWM:

1) The sector in which the tip of the reference sector is situated is to be determined from the instantaneous phase references Va *, Vb * and Vc*

- Va *, Vb *, Vc * The three pahse voltages are transformed to two phase using parks transformation.
- $v\alpha, v\beta \Theta = tan 1(v\beta/v\alpha)$
- $\alpha = \Theta$ k(60⁰); k such that $\alpha < 60^{\circ}$
- Sector number = k + 1

2) Computation of T1 and T2; here lookup tables are needed to know the values of Sin (60^{0} - α) and Sin α

3) Determination of switching vectors.

Using the corresponding sector information the actual switching time for each inverter leg is generated from the combination of effective times and zero sequence time. Equating volt-seconds along the α -axis:

$$(IVsrIcos\alpha)*Ts = Vdc *T1 + (Vdccos60^{0}) *$$

Equating volt-seconds along the β -axis:

Ts

 $(IVsrIsin\alpha) * Ts = (Vdcsin60^{\circ}) *T2$

Solving the above two simultaneous equations, one gets:

$$T_1 = \frac{|\mathbf{v}_{sr}| T_s \sin(\pi/3 - \alpha)}{V_{dc} \sin(\pi/3)}$$
$$T_2 = \frac{|\mathbf{v}_{sr}| T_s \sin\alpha}{V_{dc} \sin(\pi/3)}$$

 $|\mathbf{V}_{sr}|$ represents the length of the reference Vector and α is measured from the start of the vector. 4) Assert the appropriate control signals to affect the required switching action.







Fig.9 Space vector Simulink block



Fig10. Three phase to two phase conversion

www.ijera.com



Fig.11 Three phase voltages of conventional VSI



E. Sai Prateek et al Int. Journal of Engineering Research and Applications ISSN : 2248-9622, Vol. 4, Issue 5(Version 7), May 2014, pp.99-105



Fig.13 Three phase voltages of Z-Source inverter



Fig.14 THD Analysis of Z-source inverter voltages

| P a g e

IV. CONCLUSION

The DC bus utilisation is increased by space vector pulse width modulation.IN this paper space vector pwm is implemented for conventional voltage source inverter and zsource inverter. The z impedance network when used in gives desired output voltage and harmonic content is reduced. The space vector is implemented and corresponding results are analysed.

REFERENCES

- F. Z. Peng "Z-Source Inverter", *IEEE Trans. Ind. Appl.*, vol. 39,March-April 2003, pp. 504-510.
- [2] F. Z. Peng, X. Yuan, X. Fang and Z. Qian "Z-Source Inverter for Adjustable Speed Drives", *IEEE Trans. Power Electr. Letters*, vol. 1, No. 2, June 2003, pp. 33-35.
- [3] F. Z. Peng "Z-Source Inverter for Motor Drives", 35th Annual IEEE Power Electronics Conference, pp. 249-254.
- [4] F. Z. Peng, M. Shen and Z. Qian "Maximum Boost Control of the ZSource inverter", 35th Annual IEEE Power Electronics Conference, pp. 255-260.
- [5] P. C. Loh, D. M. Vilathgamuwa, Y. S. Lai, G. T. Chua and Y. Li "Pulse-Width Modulation of Z-Source Inverters", *Conf. Rec. IEEEIASAnnu. Meeting*, 2004, pp.148-155.
- [6] N. Muntean, L. Tutelea, I. Boldea "A Modified Carrier – Based PWM Modulation Technique in Z - Source Inverters" *IEEE Trans. Ind. Appl.*, vol. 43,March-April 2007, pp. 704-710
- [7] Arturo A. Arias M. and Wilfried Hofmann "Carrier-Based PWM for Z-Source Inverters" *IEEE Trans. Ind. Appl.*, vol. 49, 2012, pp. 504-510
- [8] Bengi Tolunay"Space Vector Pulse Width Modulation for Three-LevelConverters - a LabVIEW Implementation", UPTEC E12001